Negar Neda

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Education

New York University, Tandon School of Engineering *Sep. 2021 -2026*
PhD in Electrical and Computer Engineering, Advisor: Brandon Reagen
Thesis title: Accelerating Homomorphic Encryption Implementation

University of Tehran (UT), Tehran, Iran *Sep. 2018 - Feb. 2021*
M.Sc. in Computer Architecture, Cumulative GPA: 3.63/4
Thesis title: FPGA-based Multi-precision Accelerator for Deep Neural Networks

Amirkabir University of Technology (AUT), Tehran, Iran *Sep. 2014 - Sep. 2018*
B.Sc. in Computer Architecture, Cumulative GPA: 3.62/4
Thesis title: Implementation of a Tracking System Using LoRaWAN Protocol

Interests

· Hardware Accelerators · Privacy-preserving ML Alg. · FPGA · Homomorphic Encryption

Relevant Courses

· Computing Systems Architecture · Intro to Cryptography · Hardware Security · Machine Learning
· Neural Networks · Multicore Embedded Systems · VLSI Systems Design

Publications

· "CiFlow: Dataflow Analysis and Optimization of Key Switching for Homomorphic Encryption", IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), **N. Neda**, A. Ebel, B. Reynwar, B. Reagen, 2024.

· "Quantifying the Overheads of Modular Multiplication", IEEE International Symposium on Low Power Electronics and Design (ISLPED), D. Soni, M. Nabeel, **N. Neda**, et al., 2023.

· "Towards fast and scalable private inference", Proceedings of the 20th ACM International Conference on Computing Frontiers, J. Mo, K. Garimella, **N. Neda**, A. Ebel, B. Reagen, 2023.

· "RPU: The Ring Processing Unit", IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), **N. Neda**, D. Soni, et al., 2023.

· "Multi-Precision Deep Neural Network Acceleration on FPGAs", Asia and South Pacific Design Automation Conference (ASP-DAC), **N. Neda**, et al., 2022.

Research Experience

Graduate Research Assistant, *New York University* 2021 - Present
· Doing research on the design of hardware accelerators for **privacy-preserving machine learning** algorithms, with a focus on **Homomorphic Encryption** (HE).

Research Assistant, *University of Tehran* 2018 - 2021
·Implemented an FPGA-based Multi-precision accelerator for DDNs.

Undergrad Researcher, *Amirkabir University of Technology* 2017 - 2018
· Designed Amirkabir University of Technology IoT Gateway.

Teaching Experience

· Computing Systems Architecture · Computer Aided Digital System Design · Logic Circuit Laboratory
· Digit Design Automation

Selected Projects

• **Hardware Accelerator for Torus Fully Homomorphic Encryption (TFHE)** 2024 - ongoing

· Developing an optimized **ASIC** chiplet design for TFHE Bootstrapping by leveraging **computational parallelism** and algorithmic enhancements for improved performance and efficiency.

• **Optimized Key-Switching Dataflow for Efficient Homomorphic Encryption (HE)** 2023

· Enhanced Data Reuse by stratigically scheduling **HE Key-Switching** instructions, achieving a 4x speedup and 12x SRAM saving by minimum off-chip data movement.

• **Novel Vector-based ISA & microarchitecture to accelerate NTT.** 2022

· Designed an **ISA**, and a **hardware accelerator** for RLWE-based workloads, achieving 1485× speedup for **NTT** over CPU with modular arithmetic support, parallel processing, and optimized programming.

• **5-Stage MIPS Processor with Pipelining.**

· Designed a 5-stage pipeline MIPS processor with C++, including a 2-bit branch predictor, and a direct/fully associative cache implementation.

• **Multi-Precision Accelerator for Deep Neural Network acceleration on FPGA** 2021

· Designed a multi-precision multiplier for **FPGA** achieving a 3-15× throughput improvement by dynamically adjusting bit-width to match precision needs.

HONOR & AWARDS

· Awarded a Student Travel Grant to present our work at ISPASS 2023 & 2024
· Earned **Future Leader Fellowship** at NYU Tandon. 2022-2024
· **Ranked Top 3 in terms of GPA**, among Computer Architecture Students in AUT 2019

Technical skills

Programming	Python(Tensorflow, PyTorch), Rust, C/C++, Java, VHDL, Verilog, SystemVerilog, Co-Design, CUDA, OpenMP, Assembly LaTeX
Tools	Visual Studio, Qt, MATLAB, Jupyter Notebook, Arduino IDE, Git
Hardware CAD Tools	Vivado, Xilinx ISE Design Suite, PSPICE, HSPICE, Modelsim

Talks

· "CiFlow: Dataflow Analysis & Optimization of Key Switching for HE", ISPASS 2024
· "RPU: The Ring Processing Unit", ISPASS 2023
· "Summary of RPU: The Ring Processing Unit ", Princeton Computer Architecture Day 2023
· "A Novel Vector ISA for Accelerating Homomorphic Encryption", TECHCON 2022

Outreaches

· Session Chair, NYU Computer Architecture Day 2024
· Staff Member, International Symposium on Computer Architecture (ISCA), NY 2022